ligital signal processing apparatus and method and ither signal generating apparatus

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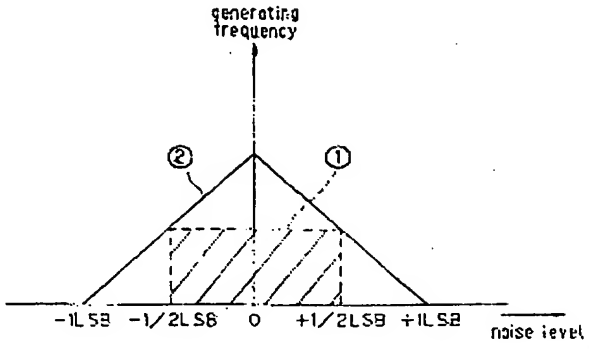
A digital signal processing apparatus and a method for carrying out a re-quantization process for turning an inputted digital signal into a digital signal with a smaller bit number includes a signal generator (10) and a re-quantization processor (13). The signal generator has a data generator (1), a delay circuit (2) and an adder (4) and generates a dither signal for which an amount of a high frequency component is larger than that of the low frequency component. The data generator (1) generates M-series data-like non-correlating data. The delay circuit (2) delays the output from the data generator (1). The adder adds (4) the output from the delay circuit and an output from the delay circuit for which the polarity has been inverted (3). In the re-quantization process, the dither signal from the signal generator and the inputted signal are added

FIG. 1



(12) and the added signal is then re-quantized (13).

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ACKGROUND

Field Of The Invention

ıe present invention relates to a digital signal processing apparatus and ethod and a dither signal generating apparatus. More particularly, the esent invention relates to a digital signal processing apparatus and ethod which employs a dither signal, and a dither signal generating pparatus.

Background of the Invention

/hen N-bit data generated by digital signal processing occurring in circuits ıch as digital filters and DSP (Digital Signal Processing) circuits are ıpplied to another signal processing sections, sometimes fraction ocessing such as rounding-down or rounding off has to be carried out on ıe lower bit data of the N-bit data so as to re-quantize the data into M bit N>M) data to ensure that the data match with the operation bit number (M ts) for the downstream signal processing sections.

is known that the data signal is added with a low level dither signal, the ıearity of the LSB (Least Significant Bit) level is increased and the tonal ıality is improved upon.

ı this case, the randomness of the noise level of the dither signal is greater the noise signal taken as the dither signal is larger. Also, a large energy vel is preferable for raising the linearity. It is, however, desirable for the ɔise level to have a distribution which at least falls within the level of one it step for the data quantization.

the dither signal noise is generated at approximately the same generating equency with respect to the noise level as shown by the relationship etween the noise level of the dither signal and the generating frequency ıdicated by the dashed line (1) shown in FIG. 1, the energy (the area for ıe inclined line) which is the dither signal cannot be made to be so large ecause the noise component for which the absolute value of the level is ırge is generated in the same way. As a result, there are therefore cases

ıere dither signals for raising the linearity do not possess sufficient ergy.Therefore, a dither signal is adopted so that the maximum nerating frequency exists where the distribution of the noise level is zero shown by the solid line (2) in Fig. 1, with the generating frequency then ducing as the absolute value for the level reduces (this kind of dither ınal will hereinafter be referred to as a distribution dither signal). In this ay, it is possible to both increase the energy and increase the linearity of e dither signal.

dither signal which has the kind of uniform characteristic shown in FIG. 2 n therefore be used so as to take into account the point of view of having frequency characteristic of a dither signal which can be added to digital ıta during re-quantization. However, this means that the noise level of ıise other than re-quantization noise is also perceptibly increased. In ırticular, when a dither signal of the necessary level is added in order to crease linearity this is accompanied by problems which go with the creasing of the noise level by 3 to 6 dB. Namely, the increasing of the ıearity is detrimental to the S/N ratio with this therefore causing a rceptible increase in the noise.

so, the kind of distribution dither signal shown by (2) in FIG. 1 is enerated by using a plurality of M-series generators 21 and 22 of the kind ıown in FIG. 3, the output of which is then added at an adder 23. Each of e M-series generators 21 and 22 therefore reciprocally output the non-ɔrrelating random data irrespective of each other. The noise data obtained y adding therefore peaks at zero level noise so as to give a level ıaracteristic where the generation frequency falls as the absolute value for ıe level becomes large. Namely, the characteristic shown by (2) in FIG. 1 obtained.

circuit of a comparatively large scale with a plurality of generators is ıerefore required in order to obtain this kind of dither signal, which resents economic problems with regards to this apparatus.

UMMARY OF THE INVENTION

is therefore an object of the present invention to provide a digital signal rocessing apparatus which resolves the aforementioned problems.

: is another object of the present invention to provide a dither signal ıenerating apparatus which resolves the aforementioned problems.

: is also a further object of the present invention to provide a digital signal ɔrocessing method which resolves the aforementioned problems.

\ccording to the present invention, there is provided a digital signal ɔrocessing apparatus which includes a signal generator, an adder, and a

-quantizer. The signal generator is for generating a dither signal having a ·ger amount of a high frequency component than that of a low frequency ·mponent. The adder is for adding a dither signal from the signal :nerator and an inputted signal. The re-quantizer is for carrying out re-ıantization processing on an output signal from the adder.

:cording to another aspect of the present invention, there is provided a ither signal generator for generating a dither signal having a larger amount a high frequency component than that of a low frequency component ıich includes a data generator and a signal generator. The data generator for generating non-correlating data. The signal generator is for generating dither signal having a larger amount of a high frequency component than at of a low frequency component by subtracting a delayed output for the ɔn-correlating data outputted from the data generator and the output from e data generator.

:cording to a still another aspect of the present invention, there is provided digital signal processing method for carrying out a re-quantization process r turning an inputted digital signal into a digital signal with a smaller bit ımber. In this method, a dither signal having a larger amount of a high :quency component than that of a low frequency component is generated / subtracting delayed non-correlating data outputted from a data generator ıd non-correlating data outputted from the data generator. A generated ther signal and an inputted dither signal are then added and the added gnal is then re-quantized.

ıerefore, according to the present invention, a signal having a frequency ıaracteristic in which the amount of the high frequency component is rger than that of the low frequency component is used as the dither signal be added to the inputted digital signal. The energy distribution for the ther energy level can therefore be made large at a band which is higher an the audible frequency band so that this can be made to be at least the ther component within the audible frequency band.This means that the fluence of the dither noise on a perceptible level can be reduced, the level the dither signal can be raised and the re-quantization linearity can :erefore be raised.

RIEF DESCRIPTION OF THE DRAWINGS

IG. 1 is a graph illustrating the distribution of the dither signal;
IG. 2 is a graph illustrating a usual dither signal characteristic;
IG. 3 is a block diagram of a usual distribution dither signal generator;
IG. 4 is a block diagram of an embodiment of a dither signal generating ɔparatus according to the present invention;
IG. 5 is a block diagram of a digital signal processing apparatus having the igital signal generating apparatus according to the present invention; and
IG. 6 is a graph illustrating the dither signal frequency characteristic

:cording to the embodiment.

ESCRIPTION OF THE INVENTION

ne following is a detailed description of a digital signal processing pparatus and a dither signal generating apparatus according to the present vention.

G. 4 is a block diagram showing a dither generator 10 according to an mbodiment of the present invention. Here, a reference numeral 1 denotes n M-series data generator for generating random data, a reference umeral 2 denotes a delay circuit such as flip-flops, a reference numeral 3 enotes a polarity inverter and a reference numeral 4 denotes an adder.

utput data from the M-series data generator 1 are supplied to the delay rcuit 2 and the polarity inverter 3. An output from the delay circuit 2 and an utput from the polarity inverter 3 are added together at the adder 4, with an utput from the adder 4 then being used as the dither signal.

ata generated at different times can be handled in the same way as data utputted from a plurality of M-series data generators because random data enerated at the M-series data generator 1 have no self-correlation except r a constant cycle data. Also, a subtractor is composed of the polarity verter 3 and the adder 4.

ccordingly, delayed data outputted at the delay circuit 2 and the data putted at the polarity inverter 3 are completely non-correlating at a point in me. A subtraction process is then carried out between two kinds of non-rrelating data by adding the outputted data which have been polarity verted with the delayed data at the adder 4.

he noise data obtained by adding (subtracting) two kinds of non-rrelating data are taken as the distribution dither signal. Namely, as nown by the solid line (2) in FIG. 1, and as mentioned above, if a zero ise level is randomly taken as the frequency peak, a level distribution naracteristic in which the generated frequency reduces as the absolute alue for the level becomes large is obtained.

he delay time for the delay circuit 2 is taken as a time which, for example, rresponds to the period of the sampling frequency Fs.

sually, data which is not at the sampling frequency usually undergoes equency filter processing via addition or subtraction. Namely, the delay me for the delay circuit 2 is made to have the period of the sampling equency Fs. Data which is then only out by the period of the sampling equency Fs is subjected to subtraction processing by the polarity inverter

and the adder 4 so that a primary high-pass filter is formed.

ither signals generated by this dither generator 10 have the kind of equency characteristic shown, for example, by the solid line A shown in IG. 6.

is also possible to arrange the polarity inverter 3 at the dither generator 10) that the polarity of the delayed data side is inverted.

IG. 5 is a block diagram showing an example of a digital signal processing)paratus having the dither generator 10 shown in FIG. 4 for carrying out -quantization from N-bit data to M-bit data. In this case, the output of the gital processor which outputs the N-bit digital data is sent to a digital ·ocessor 14 which carries out M-bit (N>M) digital processing.

amely, with respect to the N-bit data, the dither signal generated at the ther generator 10 is added at an adder 12. M-bit re-quantization ·ocessing is then carried out by rounding down or rounding off the lower ts of bit number N-M at a fraction processing circuit 13.

ne linearity of the re-quantized data can be increased by adding the dither gnal in this way and re-quantizing. In the embodiment, the noise eneration due to the dither signal occurring in the audible band is then :duced because the dither signal has the kind of frequency characteristic own by A in FIG. 6 where an amount of the high frequency component is rger than that of the low frequency component (audible frequency band)mponent). The broken line Z in FIG. 6 shows the frequency characteristic r a usual dither signal. It can be seen that the noise energy is reduced)rresponding to the hatched region within the audible band in accordance ith the dither signal A when compared with this usual example. If Fs is ken to be, for example, about 40 KHz, the audible band will be less than 2Fs.

ne problem of making the level of the dither signal larger no longer exists s a result of the noise within the audible bandwidth having been reduced. nis also means that the effect of the increase in the linearity is increased.

lso, at the dither circuit 10, it is possible to generate dither signals having e kind of characteristics shown by the dot and dashed lines B, C and D own, for example, in FIG. 6, by carrying out processing and setting the elay times at the delay circuit 2 while replacing the sampling frequency Fs ith nFs (n=2, 4, 8 . . .). In FIG. 6, the cases are shown where processing carried out for B=2Fs, C=4Fs and D=8Fs.

this way, the noise level within the audible frequency band can be :duced so that the linearity can be increased to great effect as a result of creases in the level of the dither signal.

the embodiment, the linearity of the re-quantized data is raised while at

e same time, the audible noise level is reduced. It also becomes possible generate a distribution dither signal which has a frequency peak when e noise level is zero and for which the generating frequency reduces as e absolute value for the level becomes large while using just one M-series ata generator.

so, the present invention is by no means limited to the structure of this nd of embodiment and variable modifications are possible within the cope of the claims. For example, the random data generating apparatus oes not have to be an M-series data generator. The delay circuit may also e composed a plurality of high order filters and a wide variety of settings ay be considered for the frequency characteristic of the obtained equency signal.

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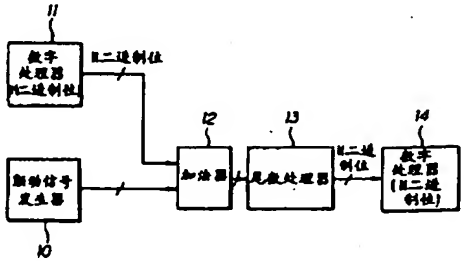
[54]发明名称 数字信号处理设备和方法及颤动信号发生设备

[57]摘要

用以进行再量化处理，将输入数字信号转换成二进制位数较小的数字信号的数字信号处理装置包括信号发生器和再量化处理器。信号发生器有数据发生器、延迟电路和加法器，产生高频分量比低频分量多的颤动信号。数据发生器产生象 M 系列数据的非相关数据。延迟电路延迟数据发生器的输出。加法器将延迟电路的输出和延迟电路极性倒换过的输出相加。再量化处理时，来自信号发生器的颤动信号和输入的信号相加，然后将相加的信号再量化。



权　　利　　要　　求　　书

1. 一种数字信号处理设备，其特征在于，它包括：

信号发生装置，用以产生高频分量比低频分量多的颤动信号；

加法装置，用以将来自所述信号发生装置的颤动信号和输入信号加起来；

再量化装置，用以对来自所述加法装置的输出信号进行再量化处理。

2. 根据权利要求1 所述的数字信号处理设备，其特征在于， 所述信号发生装置包括数据发生装置和滤波装置，数据发生装置用以产生非相关数据，滤波装置用以对从所述数据发生装置输出的非相关数据进行滤波，并输出非相关数据的高频分量。

3. 根据权利要求1 所述的数字信号处理设备，其特征在于， 所述信号发生装置包括数据发生装置、延迟装置和减法装置，数据发生装置用以产生非相关数据，延迟装置用以延迟从所述数据发生装置输出的非相关数据，减法装置用以将所述延迟装置的输出与所述数据发生装置的输出相减。

4. 根据权利要求3 所述的数字信号处理设备，其特征在于， 所述减法装置还包括极性倒换装置和加法装置，该极性倒换装置用以倒换所述数据发生装置的输出的极性，该加法装置用以将所述极性倒换装置的输出与所述延迟装置的输出加起来。

5. 一种颤动信号发生器，用以产生高频分量比低频分量多的颤动信号，其特征在于，它包括：

数据发生装置，用以产生非相关数据；

信号发生装置，用以通过将所述数据发生装置输出的非相关数据

的延迟输出与所述数据发生装置的输出相减，产生高频分量比低频分量多的颤动信号。

6.根据权利要求5 所述的颤动信号发生设备，其特征在于，所述信号发生装置包括延迟装置和减法装置，该延迟装置用以延迟所述数据发生装置的输出，该减法装置用以将所述延迟装置的输出与所述数据发生装置的输出相减。

7.根据权利要求6 所述的颤动信号发生装置，其特征在于，所述减法装置包括极性倒换装置和加法装置，该极性倒换装置用以倒换数据发生装置的输出的极性，该加法用以将所述极性倒换装置的输出与所述延迟装置的输出加起来。

8.根据权利要求6 所述的颤动信号发生装置，其特征在于，延迟装置将所述数据发生装置输出的非相关数据延迟一段相当于取样频率周期的时间。

9.一种数字信号处理方法，用以进行再量化处理，以便将输入的数字信号转换成二进制位数较小的数字信号，其特征在于所述再量化过程包括以下步骤:

将数据发生装置输出的经过延迟的非相关数据与该数据发生装置输出的非相关数据相减，从而形成高频分量比低频分量多的颤动信号;

将所产生的颤动信号与输入的颤动信号加起来；然后

对加起来之后的信号进行再量化。

10.根据权利要求9所述的数字信号处理方法，其特征在于，所述减法操作包括将所述数据发生装置输出的经延迟的非相关数据与所述数据发生装置输出的极性经过倒换的输出相加的步骤。

说　　明　　书

数字信号处理设备和方法及颤动信号发生设备

本发明涉及数字信号处理设备和方法以及颤动信号发生设备。更具体地说，本发明涉及采用颤动信号的数字信号处理设备和方法以及颤动信号发生设备。

出现在诸如数字滤波器和DSP(数字信号处理)电路之类的电路中经数字信号处理产生的N二进制位数据加到另一些信号处理部分时，有时必须对N二进制位数据的较低位数据进行诸如下舍入或舍入之类的分数处理，以便将数据重新量化成M二进制位(N>M)数据，从而确保数据与下游信号处理部分的运算位数(M二进制位)相匹配。

大家知道，这时低电平颤动信号加到数据信号上，于是LSB(最低有效位)电平的线性度提高了，从而提高了音调的质量。

在这种情况下，若用作颤动信号的噪声信号较大，则颤动信号噪声电平的随机性就较大。此外，为提高线性度，能级最好大。但噪声电平的分布最好至少在数据量化的一二进制位级电平内。

若颤动信号噪声在噪声电平方面是在与图1虚线(1)所示的颤动信号噪声电平与振荡频率之间的关系大致相同的振荡频率下产生的，则能量(斜线区域)，即颤动信号，不能取得太大，因为这时会以同样的方式产生电平绝对值大的噪声分量，从而会出现用以提高线性度的颤动信号能量不足的情况。正因为这样，所以采用了颤动信号，使出现最高振荡频率，这时如图1的实线(2)所示，噪声电平的分布为零，同时振荡频率随着电平绝对值的减小而降低(这类颤动信号以下称之为分布颤动信号)。这样，既可增加能量又能提高颤动信号的线性度。

因此可以采用特性如图2 所示地那样均匀的颤动信号，以便考虑再量化过程中可加到数字数据的颤动信号的频率特性的这种观点。但这意味着除再量化噪声外，其它噪声的噪声化电平的增加也达到可觉察出来的程度。特别是，为了提高线性度而加上电平合乎要求的颤动信号时，噪声电平的增幅一达到3至6分贝就会出问题。就是说线性度的提高对信噪比产生有害的影响，因而这样做会引起噪声显著增加。

此外，如图1中的(2)所示的那一种分布的颤动信号是采用多个图3所示的那一种M系列发生器21和22产生的，发生器的输出接着在加法器23相加。这样，各M 系列发生器21和22交替地输出彼此互不相关的非相关随机数据。于是相加得出的噪声数据在零电平噪声下达到峰值，从而使得出的电平特性的振荡频率随着电平绝对值的变大而下降。就是说，得出图1中(2)所示的特性。

因此，为获取这类颤动信号就需要具有多个发生器的规模较大的电路，这样，这种设备在经济方面就成问题。

因此本发明的目的是提供一种能解决上述问题的数字信号处理设备。

本发明的另一个目的是提供一种能解决上述问题的颤动信号发生设备。

本发明还有一个目的是提供一种能解决上述问题的的数字信号处理方法。

按照本发明提供的数字信号处理设备包括一个信号发生器、一个加法器和一个再量化器。信号发生器用以产生高频分量比低频分量多的颤动信号。加法器用以将来自信号发生器的颤动信号和输入信号相加。再量化器用以对来自加法器的输出信号进行再量化处理。

按照本发明的另一个方面，本发明提供的用以产生高频分量比低频分量多的颤动信号的颤动信号发生器包括一个数据发生器和一信号

发生器。数据发生器用以产生非相关数据。信号发生器用以通过将从数据发生器输出的非相关数据的延迟输出与数据发生器的输出相减而产生高频分量比低频分量多的颤动信号。

按照本发明的再一个方面，本发明提供了一种进行再量化处理以便将输入的数字信号转换成二进制位数较小的数字信号的方法。在该方法中，高频分量比低频分量多的颤动信号是通过将数据发生器输出的经延迟的非相关数据与数据发生器输出的非相关数据相减而产生的。接着将所产生的颤动信号与输入的颤动信号相加，再将经相加的信号进行再量化。

因此，按照本发明，准备加到所输入的数字信号的颤动信号采用频率特性中高频分量比低频分量多的信号。这样，可以使颤动能级在高于声频带的频带能量分布宽，从而至少可使它成为声频带内的颤动分量。这就是说，可以减小颤动噪声对可觉察电平的影响，可以提高颤动信号的电平，从而提高再量化的线性度。

图1是显示颤动信号分布情况的图象。

图2是一般颤动信号的特性的图象。

图3是一般分布颤动信号发生器的方框图。

图4是本发明的颤动信号发生设备一个实施例的方框图。

图5是具有本发明数字信号发生设备的数字信号处理设备的方框图。

图6是上述实施例的颤动信号频率特性的图象。

下面详细说明本发明的数字信号处理设备和颤动信号发生设备。

图4 是本发明的颤动信号发生器10的方框图。这里，编号1表示用以产生随机数据的M系列数据发生器，编号2表示诸如触发器之类的延迟电路，编号3表示极性倒换器，编号4表示加法器。

来自M系列数据发生器1的输出数据提供给延迟电路2 和极性倒换

器3。来自延迟电路2的输出和来自极性倒换器3的输出在加法器4相加，然后用加法器4的输出作为颤动信号。

在不同时间产生的数据可以按相同方式作为从多个M系列数据发生器输出的数据进行处理，因为在M系列数据发生器1产生的随机数据除了恒定周期数据外是没有自相关关系的。此外，由该极性倒换器3和加法器4构成减法器。

因此，在延迟电路2输出的延迟数据和在极性倒换器3输入的数据在某一时刻完全互不相关。接着在两种非相关数据之间进行减法操作，即，将极性经过倒换的输出数据与延迟数据在加法器4加起来。

两种非相关数据相加(相减) 得出的噪声数据就作为分布颤动信号。就是说，如图1中的实线(2)所示，且如上面说过的那样，若随机取零噪声电平作为频率峰值，就可以得出所产生的频率随着电平绝对值的变大而降低的电平分布特性。

延迟电路2的延迟时间可取例如相当于取样频率Fs的周期的时间。

通常，不处在取样频率的数据一般都要经历通过加法或减法进行的频率滤波处理。就是说，使延迟电路2的延迟时间具有取样频率Fs的周期。这时只在取样频率Fs的周期输出的数据是要由极性倒换器3和加法器4进行减法处理的，从而形成基本高通滤波器。

该颤动信号发生器10产生的颤动信号具有例如图6中实线A所示的频率特性。

此外也可以将极性倒换器3 配置在颤动信号发生器10处，以便倒换延迟数据的极性。

图5是具有图4 的颤动信号发生器10用以将N二进制位数据再量化成 M二进制位数据的数字信号处理设备一个实例的方框图。在此情况下，数字处理器输出的N 二进制位数字数据发送到数字处理器14，由数字处理器14进行M二进制位(N>M) 数字处理。

就是说，将颤动信号发生器10产生的颤动信号在加法器12中与N二进制位数据加起来。接着在分数处理电路13下舍入或舍入二进制位数为N-M的较低位，进行M二进制位再量化处理。

这样加颤动信号并进行再量化可以提高再量化数据的线性度。在实施例中，因声频带产生的颤动信号而产生的噪声由于颤动信号具有图6中A所示的高频分量比低频分量（声频带分量）多的那种频率特性而减少。图6中的虚线Z示出了普通颤动信号的频率特性。可以看到，噪声能量比起该普通实例来随颤动信号A 而减小，相当于声频带内的阴影部位。取Fs为例如大约40千赫，则声频带会小于1/2Fs。

由于声频带宽内的噪声减少了，因而再也不存在扩大颤动信号电平的问题。这也意味着提高线性度的作用提高了。

此外，在颤动信号发生电路10还可以通过处理和设定在延迟电路2的延迟时间、同时用nFs（n=2，4，8…）代替取样频率Fs，产生例如图6中所示的点划线B，C和D 的那种特性的颤动信号。图6中，可以看到这是B=2Fs、C=4Fs和D=8Fs的处理情况。

这样由于颤动信号的电平提高了，因而可以减小声频带内的噪声电平，从而有效地提高了线性度。

在上述实施例中，再量化数据的线性度提高了，同时听得到的噪声的电平降低了。此外还可以只采用一个M系列数据发生器产生噪声电平为零时频率处于峰值且振荡频率随电平绝对值的变大而降低的分布颤动信号。

此外，本发明并不局限于上述那种实施例的结构，在不脱离权利要求书的范围的前提下是可以对上述实施例作种种修改的。举例说，随机数据发生设备不一定非要M系列数据发生器不可。延迟电路也可以由多个高阶滤波器组成，得出的频率信号的频率特性也可以考虑采用各种不同的设定值。

说 明 书 附 图

图 1

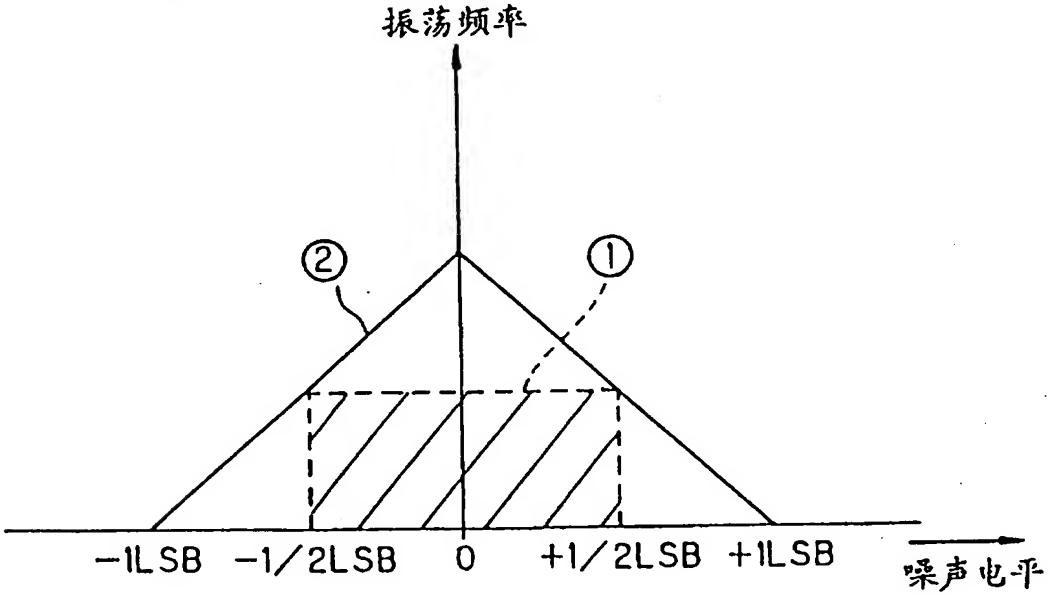


图 2

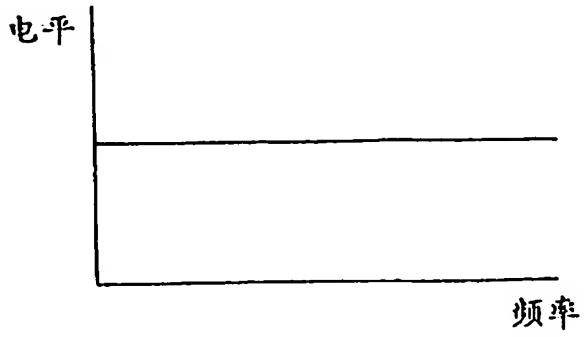


图 3

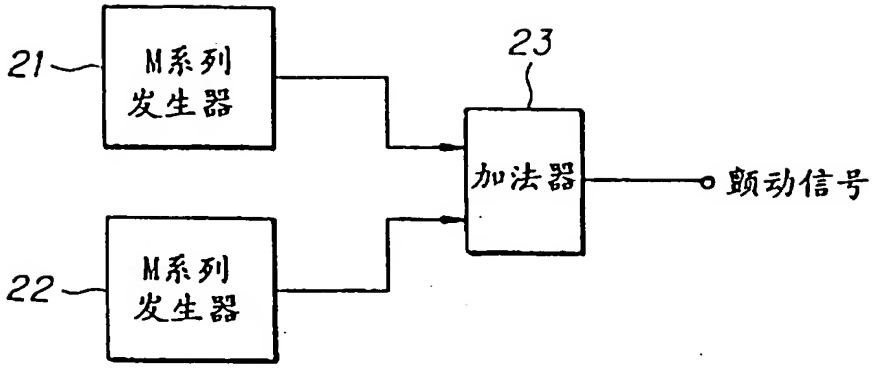

21
M系列
发生器
22
M系列
发生器
23
加法器
颤动信号

图 4

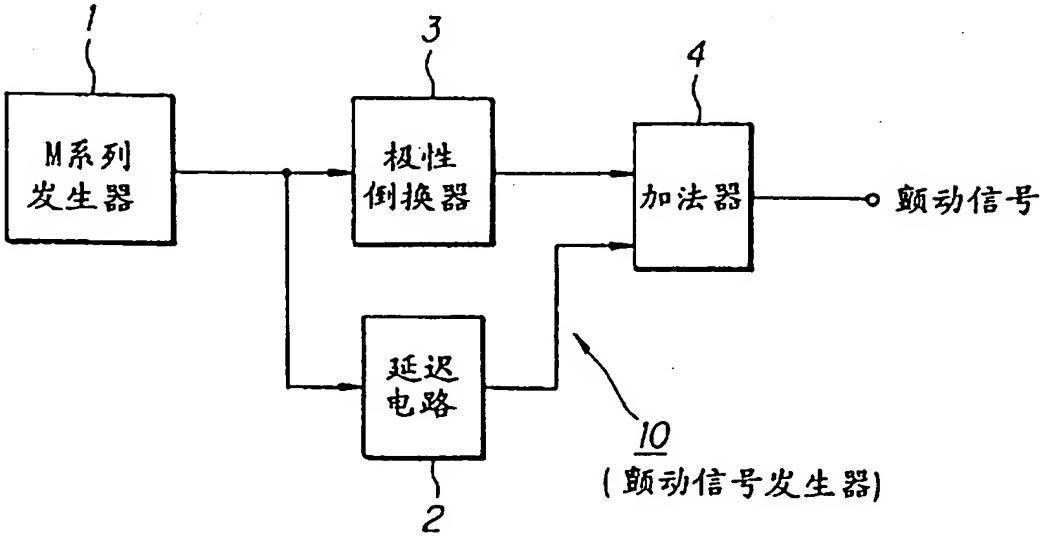

1
M系列
发生器
3
极性
倒换器
4
加法器
颤动信号
延迟
电路
2
10
(颤动信号发生器)

图 5

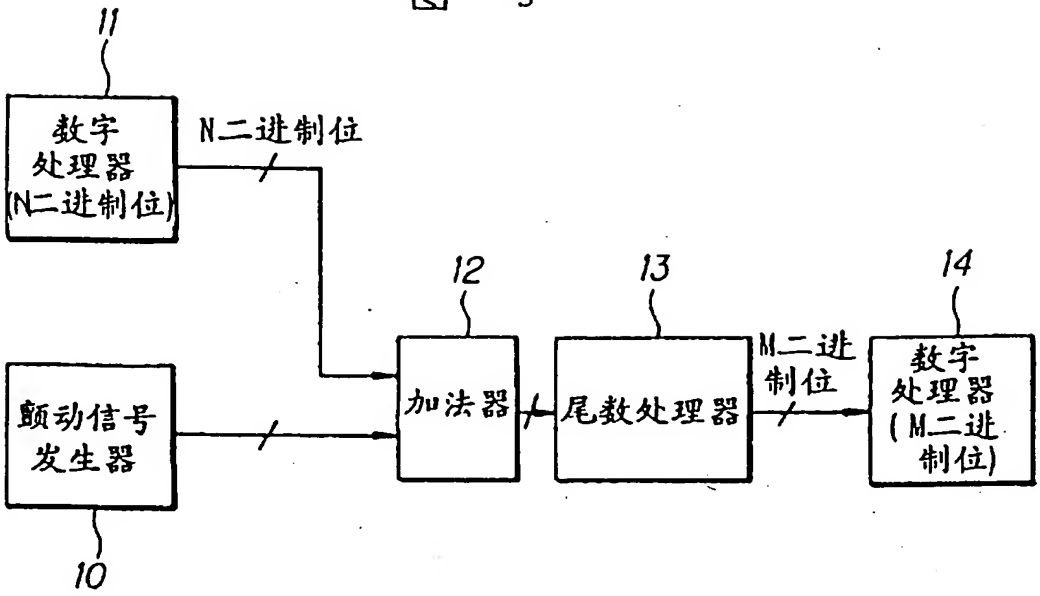
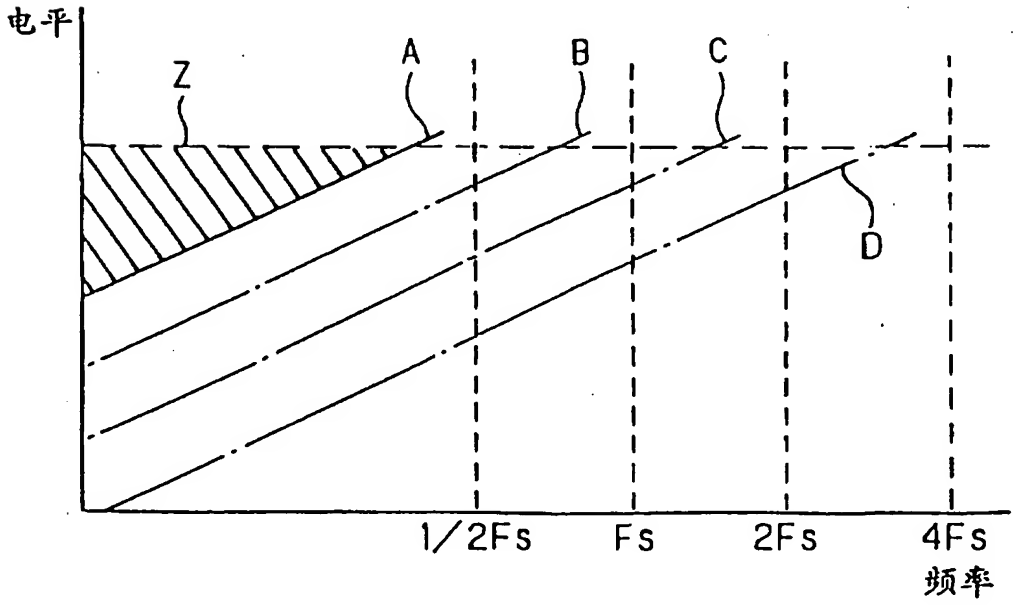

11
数字处理器(N二进制位)
N二进制位
12
13
14
加法器
尾数处理器
M二进制位
数字处理器(M二进制位)
颤动信号发生器
10

图 6


电平
Z
A
B
C
D
1/2Fs
Fs
2Fs
4Fs
频率